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ABSTRACT OF THE DISCLOSURE

In a high-voltage MOS transistor, source/drain offset regions have the same dopant concentration and the same diffusion depth but the length **Ls** of the source offset region is set greater than the length **Ld** of the drain offset region. Accordingly, the resistance value of the source offset region increases, thus raising a source voltage **VS**, too. As a result, a substrate voltage **VW** minus a forward biased breakdown voltage of silicon can be kept equal to or less than the source voltage **VS** more easily, and therefore, a sustaining breakdown voltage of the transistor can be increased.

SUB C1